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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,238	INOUE ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/02/2008, 03/28/2008 AND 05/23/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-55 are pending for examination.

2. Claim 29 is objected to because it is directed to a method claims but it is dependent on an apparatus claim 27, hence it is directed to both a method and an apparatus claim. The claim should be either method or apparatus claim, and not both. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood:

i. As per claim 1, line 11, it is not clearly understood whether " at least one processor task" is one of the selected processor task? line 13, it is not clearly understood whether "the selected task" is the same as " processor task" referred in line 11 or different tasks?

ii. As per claim 10, it has the same deficiency as claim 1.

iii. As per claim 21, lines 21, it is unclear whether the plurality of processor task are being executed or the processor tasks are in the processor queue?

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-16, 21-23, 25-38, 43-47 and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bahr et al. (EP 0459931 A2), in view of Susuki et al. (US 4,394,730).

As per claim 1, Bahr teaches the invention substantially as claimed including a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of processing units coupled to and for accessing a shared memory (abs., lines 1-3), the method comprising:

providing that selected processor tasks for execution and having respective priorities be copied from the shared memory to one or more of the processing units, and that each of the selected tasks is executed at one of the processing units (col. 6, lines 27-31).

7. Bahr doesn't explicitly teach migrating at least one processor task being executed at a first from one of the processing units from the first processing unit, based on priority of the selected tasks, to another of the processing units. However, Susuki teaches migrating at least one

processor task being executed at a first from one of the processing units from the first processing unit, based on priority of the selected tasks, to another of the processing units (abs., lines 1-14; wherein, transferring tasks from one processing unit to another is migrating the task as claimed).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bahr and Susuki because Susuki teaching of migrating from one processing unit to another based on priority of the selected tasks which would improve system performance and system load balancing whenever needed.

9. As per claim 2, Bahr doesn't explicitly teach that prohibiting the execution of the processor task from the shared memory after the copying of the processor task to one or more of the processing units (col. 6, lines 40-45; col. 6, lines 50-53).

10. However, it would have been obvious to one of ordinary skill in the art a the time the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilizes this concept to improve overall memory access efficiency

11. As per claim 3, Bahr teaches the plurality of processing units comprises a main processor unit and a plurality of sub-processing units, each of the plurality of sub-processing units having a local memory (col. 6, lines 40-42), and wherein the processor tasks are copied to local memory

and executed in local memory (col. 6, lines 40-42; col. 6, lines 50-53).

12. As per claim 4, Susuki teaches migration of the at least one processor task is based on a condition (abs., lines 1-8).

13. As per claim 5, Susuki teaches the condition is based on respective priority levels associated with the processor tasks (abs., lines 1-8).

14. As per claim 6, the combined teaching doesn't explicitly teach that satisfaction of the condition and the initiating of the migration is not based on preemptive action. However, it is obvious that the migration is not based on preemption since the tasks returned to the processor where they were migrated from once the condition is ended.

15. As per claim 7, Bahr teaches requiring that the sub-processing units select processor tasks from the shared memory for execution based on their priority levels.

16. As per claim 8, Bahr teaches requiring that the sub-processing units select a processor task of higher priority before a processor task of lower priority from the shared memory (col. 7, lines 23-26; col. 8, lines 15-16; col. 9, lines 29-30).

17. As per claim 9, Bahr teaches selecting a first processor task of a first priority level from the shared memory for execution by a first sub-processing unit;

selecting a second processor task of a second priority level from the shared memory for execution by a second sub-processing unit (col. 3, lines 14-27; col. 9, lines 29-30); and

yielding the first sub-processing unit to a third processor task of a third priority level before completing the execution of the first processor task, the third processor task being selected because its priority level is higher than any other processor tasks that are ready to be executed (col. 1, lines 26-28).

As per claim 10, bahr teaches a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of processing units coupled to and for accessing a shared memory(col. 1-3), the method comprising:

providing that selected processor tasks for execution and having respective priorities be copied from the shared memory to one or more of the processing units, and that each of the selected tasks is executed at one of the processing units (col. 6, lines 27-31);

providing that the processing units select processor tasks from the shared memory for execution based on the priority levels of the processor tasks (col. 1, lines 12-14; col. 1, lines 28-30);

18. Bahr doesn't explicitly teach that migrating a processor task of lower priority running on a first of the processing units from the first processing unit, based on priority of the selected tasks, to another of the processing units; and after the migrating, providing that the first processing unit run a processor task having a higher priority than the migrated, lower prior

processor task.

19. However, Susuki teaches migrating a processor task of lower priority running on a first of the processing units from the first processing unit, based on priority of the selected tasks, to another of the processing units; and after the migrating, providing that the first processing unit run a processor task having a higher priority than the migrated, lower prior processor task (abs., lines 1-14).

20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bahr and Susuki because Susuki teaching of migrating from one processing unit to another based on priority of the selected tasks which would improve performance and system load balancing whenever needed.

21. As per claim 11, Bahr doesn't explicitly teach prohibiting the execution of the processor task from the shared memory after the copying of the processor task to one or more of the processing units.

22. However, it would have been obvious to one of ordinary skill in the art a the time the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilizes this concept to improve overall memory access efficiency

23. As per claim 12, Bahr teaches the plurality of processing units comprises a main processor unit and a plurality of sub-processing units, each of the plurality of sub-processing units having a local memory (abs. lines 1-3), and wherein the processor tasks are copied to local memory and executed in local memory (col. 6, lines 40-42; col. 6, lines 50-53).

24. As per claim 13, Bahr teaches requirement that the sub-processing units select a processor task of higher priority before a processor task of lower priority from the shared memory (col. 7, lines 23-26; col. 8, lines 15-16; col. 9, lines 29-30).

25. As per claim 14, Bahr teaches selecting a plurality of processor tasks of associated priority levels from the shared memory, based on the priority levels, for execution by a number of sub-processing units (col. 7, lines 23-27);

causing an n-th processor task in the shared memory having a given priority level to become ready for execution; and

determining whether the given priority level is higher than any of the priority levels of the plurality of processor tasks whose execution has not been completed(col. 1, lines 22-25).

26. As per claim 15, Bahr teaches that at least one of the sub-processing units is operable to perform the determination (col. 1, lines 22-25).

27. As per claim 16, Bahr teaches preemptively replacing one of the plurality of processor tasks of lower priority level than the given priority level with the n-th processor task(col. 1, lines

22-28).

28. As per claim 21, Bahr teaches A method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of sub-processing units and a main processing unit coupled to and for accessing a shared memory, each sub-processing unit including an on-chip local memory separate from the shared memory (abs., lines 1-3; col.1, lines 49-51), the method comprising:

providing that the processor tasks for execution and having respective priorities be copied from the shared memory into the local memory of the sub-processing units and that each of the tasks is executed at one of the sub-processing units(col. 6, lines 27-31).

selecting a plurality of processor tasks of associated priority levels from the shared memory for execution by one or more of the sub-processing units (col. 7, lines 23-27);

providing that the sub-processing units determine whether an n-th processor task in the shared memory having a given priority level has a higher priority level than any of the priority levels of the plurality of processor tasks (col. 1, lines 22-28).

29. Bahr doesn't explicitly teach migrating at least one processor task being executed at a first of the sub-processing units from the first sub-processing unit, based on priority of the task being executed at the first sub-processing unit, to another of the sub-processing units and prohibiting the execution of the processor tasks from the shared memory after the copying into the local memory of the sub-processing units.

30. However, Susuki teach migrating at least one processor task being executed at a first of the sub-processing units from the first sub-processing unit, based on priority of the task being executed at the first sub-processing unit, to another of the sub-processing units (abs., lines 1-14).

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bahr and Susuki because Susuki teaching of migrating from one processing unit to another based on priority of the selected tasks which would improve system performance and system load balancing whenever needed.

32. The combined teaching doesn't explicitly teach that prohibiting the execution of the processor tasks from the shared memory after the copying into the local memory of the sub-processing units.

33. However, it would have been obvious to one of ordinary skill in the art a the time the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilizes this concept to improve overall memory access efficiency

34. As per claim 22, Bahr teaches that a processor task of lower priority running on one of the sub-processing units is preemptively replaced with a processor task of higher priority (col.1, lines 22-28).

35. As per claim 23, Bahr teaches that the sub-processing units use a shared task priority table in determining whether the n-th processor task is of a higher priority level than the plurality of processor tasks (col. 1, lines 19-25).

36. As per claim 25, Bahr teaches that a sub-processing unit, when seeking to determine whether the n-th processor task is of a higher priority level than the plurality of processor tasks, searches the shared task priority table to find an entry pair indicating a lower priority level (col. 1, lines 23-26; col. 3, lines 14-16; col. 7, lines 25-26).

37. As per claim 26, Bahr teaches a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of sub-processing units and a main processing unit coupled to and for accessing a shared memory, each processing unit including an on-chip local memory separate from the shared memory (abs., lines 1-3), the method comprising:

providing that the processor tasks for execution and having respective priorities be copied from the shared memory into the local memory of the sub-processing units and that each of the tasks is executed at one of the sub-processing units (col.6, lines 27-31) and

providing that the sub-processing units select processor tasks from the shared memory for execution based on priority levels of the processor tasks(col. 7, lines 23-27).

38. Bahr doesn't explicitly teach prohibiting the execution of the processor tasks from the shared memory after the copying into the local memory of the sub-processing units; and

migrating a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor task of lower priority in response to an interrupt received by the given sub-processing unit.

39. However Susuki teaches migrating a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor task of lower priority in response to an interrupt received by the given sub-processing unit (abs., ,lines 1-14).

40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bahr and Susuki because Susuki teaching of migrating from one processing unit to another based on priority of the selected tasks which would improve system performance and system load balancing whenever needed.

41. The combined teaching doesn't explicitly teach prohibiting the execution of the processor tasks from the shared memory after the copying into the local memory of the sub-processing units. However, it would have been obvious to one of ordinary skill in the art a the time the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilizes this concept to improve overall memory access efficiency

42. As per claim 27, Bahr teaches a multi-processor apparatus, comprising:

a plurality of processing units, each processing unit including local memory in which to execute processor tasks (abs., lines 1-3; col.6, lines 50-53); and

a shared memory operable to store processor tasks that are ready to be executed and have respective priorities, wherein:

the processor tasks are copied from the shared memory into the local memory of the processing units for execution of the processor tasks by the processing units (col.6, lines 50-53).

43. Bahr doesn't explicitly teach at least one processor task being executed at a first of the processing units is migrated from the first processing unit, based on priority of the tasks ready to be executed, one of the processing units to another of the processing units.

44. However, Susuki teaches at least one processor task being executed at a first of the processing units is migrated from the first processing unit, based on priority of the tasks ready to be executed, one of the processing units to another of the processing units (abs., lines 1-14).

45. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bahr and Susuki because Susuki teaching of migrating from one processing unit to another based on priority of the selected tasks which would improve system performance and system load balancing whenever needed.

46. As per claim 28, Bahr doesn't explicitly teach prohibiting the execution of the processor task from the shared memory after the copying of the processor task to the local memory of the processing units.

47. However, it would have been obvious to one of ordinary skill in the art a the time the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilize this concept to improve overall memory access efficiency.

48. As per claim 29, Bahr teaches the plurality of processing units comprises a main processor unit and a plurality of sub-processing units, each of the plurality of sub-processing units having a local memory, and wherein the processor tasks are copies to local memory and executed in local memory (abs., lines 1-3; col. 6, lines 40-46).

49. As per claim 30, it is the apparatus claim of the method claim 4. Therefore, it is rejected for the same rational as claim 4.

50. As per claim 31, Susuki teaches the condition is based on respective priority levels associated with the processor tasks (abs., lines 1-14).

51. As per claim 32, it is the apparatus claim of the method claim 6. Therefore, it is rejected for the same rational as claim 6.

52. As per claim 33, Bahr teaches the sub-processing units are operable to select processor tasks from the shared memory for execution based on their priority levels (col.1, lines 19-28; col. 3, lines 14-16).

53. As per claim 34, Bahr teaches the sub-processing units are operable to select a processor task of higher priority before a processor task of lower priority from the shared memory (col.7, lines 23-27).

54. As per claim 35, it is the apparatus of claim of claim 9. Therefore, it is rejected for the same reason as claim 9.

55. As per claim 36, Bahr teaches the sub-processing units are operable to:

select a plurality of processor tasks of associated priority levels from the shared memory for execution (col. 7, lines 23-27); and

determine whether an n-th processor task in the shared memory having a given priority level that has become ready for execution at one of the sub-processing units has a higher level priority than any of the priority levels of the plurality of processor tasks whose execution has not been completed (col. 1, lines 24-28).

56. As per claim 37, Bahr teaches at least one of the sub-processing units is operable to perform the determination (col. 1, lines 24-28).

57. As per claim 38, Bahr teaches at least one of the sub-processing units is operable to preemptively replace one of the plurality of processor tasks of lower priority level than the given priority level with the n-th processor task (col.1, lines 24-28).

58. As per claim 43, Bahr teaches A multi-processor apparatus, comprising:

a plurality of sub-processing units, each sub-processing unit including an on-chip local memory and for executing processor tasks (abs. Lines 1-2); and

a shared memory operable to store processor tasks having respective priorities and that are ready to be executed (abs. Lines 2-3; col. 7, lines 23-37), wherein:

the processor tasks are copied from the shared memory into the local memory of the sub-processing units for execution by the sub-processing units and the processor tasks are not executed from the shared memory (col.6, lines 35-42),

the sub-processing units are operable to select processor tasks from the shared memory for execution based on the priority levels of the processor tasks(col.7, lines 25-27; col.8, lines 14-16; col. 9, lines 29-30).

59. Bahr doesn't explicitly teach that at least one of the sub-processing units is operable to migrate a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor task of lower priority in response to an

interrupt received by the given sub-processing unit.

60. However, Susuki teaches that at least one of the sub-processing units is operable to migrate a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor task of lower priority in response to an interrupt received by the given sub-processing unit (abs., lines 1-14).

61. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bahr and Susuki because Susuki teaching of migrating from one processing unit to another based on priority of the selected tasks which would improve system performance and system load balancing whenever needed.

62. As per claim 44, Bahr teaches the sub-processing units are operable to select a processor task of higher priority before a processor task of lower priority from the shared memory (col.9, lines 29-30).

63. As per claim 45, Bahr teaches the sub-processing units are operable to:

select a plurality of processor tasks of associated priority levels from the shared memory for execution (col. 1, lines 22-30; col. 23, lines 14-17)

64. Bahr doesn't explicitly teach determine which of the plurality of processor tasks running on the sub-processing units has a lowest priority level that is lower than the priority level of the

processor task running on the given sub-processing unit (abs., lines 1-14).

65. As per claim 46, Bahr teaches the given sub-processing unit is operable to perform the determination (col.1, lines 22-30).

66. As per claim 47, Susuki teaches the given processor task is migrated to the sub-processing unit running the processor task of lowest priority level (abs., lines 1-14).

67. The combined teaching doesn't explicitly teach replacing that processor task. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude the replacement to the processor task upon migration for task that need special attention at the time.

68. As per claim 51, the combined teaching doesn't explicitly teach the yielding sub-processing unit is operable to copy the given processor task of higher priority from the local memory of the given sub-processing unit into its local memory for execution.

69. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude that the yielding sub-processing unit is operable to copy the given processor task of higher priority from the local memory of the given sub-processing unit into its local memory for execution which is obvious in order to prepare the task to be executed on the migrated processor, the task has to be copied from the processing unit where it is migrated

from to the processing unit to which it is migrated.

70. As per claim 52, Bahr teaches the given sub-processing unit is operable to use a shared task priority table in determining which processor task is of the lowest priority level (col. 3, lines 14-16; col.7, lines 25-26).

71. Claims 17-20, 24, 39-42, 48-50 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bahr et al. (EP 0459931 A2), in view of Susuki et al. (US 4,394,730) and further in view of Gaetner (US5,452,452).

72. As per claim 17, the combined teaching of Bahr and Susuki doesn't explicitly teach a first of the sub-processing units is operable to at least initiate the replacement and cause another of the plurality of sub-processing units to yield execution of a processor task of lower priority level.

73. However, Gaetner teaches a first of the sub-processing units is operable to at least initiate the replacement and cause another of the plurality of sub-processing units to yield execution of a processor task of lower priority level (col.6, lines 64-67; col. 8, lines 1-5).

74. It would have been obvious to one of ordinary skill in the art to combine Bahr, Susuki and Gaetner because Gaetner teaching of initiation of the replacement and cause another of the plurality of sub-processing units to yield execution of a processor task of lower priority level

would improve the overall system efficiency by executing tasks that require immediate attention.

75. As per claim 18, Gaetner teaches that providing that the initiating first_sub-processing unit issues an interrupt to the yielding, another sub-processing unit in order to initiate the replacement of the processor task of lower priority level (col.6, lines 64-67; col. 8, lines 1-5).

76. As per claim 19, Bahr teaches providing that the yielding sub-processing unit writes the processor task of lower priority from its local memory back into the shared memory (col. 6, lines 31-33).

77. As per claim 20, Bahr teaches providing that the yielding sub-processing unit copies the n-th processor task of higher priority from the shared memory into its local memory for execution (col. 1, lines 24-28; col. 7, lines 23-26).

78. As per claim 24, the combined teaching doesn't explicitly teach that the shared task priority table includes entry pairs of sub-processing unit identifiers and processor task priority identifiers; and each entry includes a sub-processing unit identifier and priority identifier pair that indicates a priority level of a given processor task running on an associated sub-processing unit.

79. However, Gaetner teaches that the shared task priority table includes entry pairs of sub-processing unit identifiers and processor task priority identifiers; and each entry includes a sub-

processing unit identifier and priority identifier pair that indicates a priority level of a given processor task running on an associated sub-processing unit(col. 4, lines 6-13; col. 5, lines 23-25).

80. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the shared task priority table such that the entry pairs are current which would improve system scheduling by having an updated records of each task and its current priority.

81. As per claim 39, it is the apparatus claim of the method claim 17. Therefore, it is rejected under the same rational.

82. As per claim 40, Gaetner teaches the initiating sub-processing unit is operable to issue an interrupt to the yielding sub-processing unit in order to initiate the replacement of the processor task of lower priority level (col.6, lines 64-67; col. 8, lines1-5).

83. As per claim 41, Bahr teaches the yielding sub-processing unit is operable to write the processor task of lower priority from its local memory back into the shared memory (col.1, lines 26-28; col. 6, lines 31-33).

84. As per claim 42, Bahr teaches the yielding sub-processing unit is operable to copy the n-th processor task of higher priority from the shared memory into its local memory for execution

(col. 1, lines 22-28; col. 7, lines 23-27).

85. As per claim 48, the combined teaching doesn't explicitly teach the given sub-processing unit is operable to at least initiate the migration and causing the sub-processing unit running the processor task of lowest priority level to yield execution to the given processor task of higher priority level.

86. However, Gaetner teaches the given sub-processing unit is operable to at least initiate the migration and causing the sub-processing unit running the processor task of lowest priority level to yield execution to the given processor task of higher priority level (col.6, lines 64-69; col. 8, lines 1-5).

87. As per claim 49, Gaetner teaches the given sub-processing unit is operable to issue an interrupt to the yielding sub-processing unit in order to initiate the replacement of the processor task of lowest priority level (col.8, lines 1-5).

88. As per claim 50, Bahr teaches the yielding sub-processing unit is operable to write the processor task of lowest~ priority from its local memory back into the shared memory (col. 1, lines 24-28).

89. As per claim 53, it is the apparatus claim of the method claim 24. Therefore, it is rejected under the same rational.

90. As per claim 54, Bahr teaches the given sub-processing unit is operable to search the shared task priority table to find an entry pair indicating a lowest priority level (col.3, lines 14-16; col. 7, lines 25-26).

91. As per claim 55, the combined teaching doesn't explicitly teach the sub-processing units are operable to modify the shared task priority table such that the entry pairs are current.

92. However, Gaetner teaches the sub-processing units are operable to modify the shared task priority table such that the entry pairs are current (col. 4, lines 6-13; col. 5, lines 23-25).

93. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the shared task priority table such that the entry pairs are current which would improve system scheduling by having an updated records of each task and its current priority.

Response to Arguments

94. Applicant's arguments with respect to claim1-55 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

95. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

96. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

97. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

98. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

99. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Caroline Arcos/
Examiner, Art Unit 2195